

What is claimed is:

1. A data read circuit in a semiconductor device,
comprising:

selection means for selectively reading output
5 data from a plurality of circuit blocks to shared data
lines;

precharging means for precharging said shared
data lines;

determination means for determining whether
10 said output data that have been read are to be supplied
as output to the outside in accordance with a
determination start signal that is synchronized with a
selection signal for said selection means; and

discharging means for being controlled by the
15 determination result of said determination means, and
being inserted in a cascade connection in data lines that
are shared with a succeeding circuit block;

whereby a control operation that if, based on
the determination result, the output data that are to be
20 transferred are at a low level, said discharging means is
placed in a conductive state to discharging the shared
data lines for the succeeding circuit block, and if the
data that are to be transferred are at a high level, the
shared data lines for the succeeding circuit block is
25 precharged with said precharging means, is successively
executed, as far as the lowest-order circuit block, to

thereby supply data of a logic level that corresponds to said output data as output.

2. A data read circuit according to claim 1,
5 wherein:
said circuit block is a bank block of a memory circuit;
said selection means comprises a row decoder, horizontal lines, and a column decoder;
10 said selection signal is a horizontal line;
and
said shared data lines are vertical lines.

3. A data read circuit in a semiconductor device,
15 comprising:
a plurality of banks each having multiport memory cells for transferring data of each memory cell through a single bit line in accordance with a single-end scheme;
20 determination means for determining, in accordance with a determination start signal that is synchronized with a word line signal, whether data in each bank that are read to said single bit line are to be supplied as output to the outside;
25 discharging means that enters a conductive state when the determination result of said determination

means indicate that output is possible, for discharging the bit line of the succeeding bank;

precharging means for precharging said bit line; and

5 read means that is interposed between said banks;

whereby a control operation, based on the determination result of said determination means of this particular bank, for determining whether data transfer
10 by said read means in the succeeding bank is allowed, is successively executed, as far as the lowest-order bank, to perform a desired data transfer.

4. A data read circuit of a semiconductor device,
15 comprising:

a plurality of banks each having multiport memory cells for transferring data of each memory cell through a single bit line in accordance with a single-end scheme; and

20 read means that is interposed between said banks for supplying as output to the outside data that have been read to a single bit line for each of said banks;

said read means including:

25 a single NOR means for receiving as input said data and a determination start signal for determining, in

synchronization with a word line signal, whether said data are to be transferred; and

discharging means for discharging the lower-order bit line in accordance with the output result of the NOR means;

whereby a control operation, based on the determination result of said NOR means of this particular bank, for determining whether data transfer by said read means in the succeeding bank is allowed, is successively executed, as far as the lowest-order bank, to thereby perform a desired data transfer.

5. A data read circuit in a semiconductor device, comprising:

a plurality of banks having read-only memory cells for transferring data of each cell through a single bit line; and

read means that is interposed between said banks for supplying data that have been read to a single bit line for each of said banks as output to the outside;

said read means including:

a single NOR means for receiving as input said data and a determination start signal for determining, in synchronization with a word line signal, whether said data are to be transferred; and

discharging means for discharging the lower-

order bit·line·in accordance with the output result of
said NOR means;

whereby a control operation, based on the
determination result of said NOR means of a particular
5 bank, for determining whether data transfer by said read
means of the succeeding bank is allowed, is successively
executed, as far as the lowest-order bank, to thereby
perform execute the desired data transfer.

10 6. A data read circuit in a semiconductor device,
comprising:

a plurality of banks each constituted by
predetermined logic circuits;

data output lines provided inside each of said
15 banks;

wired OR circuits in which transistors each
controlled by a predetermined input signal are connected
by wired OR to said data output lines; and

read means interposed between said banks for
20 reading output data of said wired OR circuits to the
outside;

said read means including:

a single NOR means for receiving as input said
output data and a determination start signal that is of
25 the opposite phase of a precharging signal to precharge
said data line for determining whether or not said output

data are to be transferred; and

discharging means for discharging a lower-order data output line in accordance with the output result of the NOR means;

5 whereby a control operation, based on the determination result of said NOR means of this particular bank, for determining whether data transfer by said read means in the succeeding bank is allowed, is successively executed, as far as the lowest-order bank, to thereby
10 perform a desired data transfer.

7. A data read circuit of a semiconductor device, comprising:

 a plurality of banks each having multiport
15 memory cells for transferring data of each memory cell through a single bit line in accordance with single-end scheme; and

 read means that is interposed between said banks for supplying as output to the outside data that
20 have been read to a single bit line for each of said banks;

 said read means including:

 a clocked inverter for supplying as output said data when a determination start signal, which is
25 synchronized with a word line signal, for determining whether or not said data are to be transferred is in an

active state; .

discharging means for discharging the lower-order bit line in accordance with the output result of said clocked inverter; and

5 discharge prevention means for preventing the discharging operation of said discharging means and holding the input of said clocked inverter at a precharged potential when said determination start signal is in an inactive state;

10 whereby a control operation, based on the output result of said clocked inverter of this particular bank, for determining whether data transfer by said read means in the succeeding bank is allowed, is successively executed, as far as the lowest-order bank to thereby
15 perform a desired data transfer.

8. A data read circuit in a semiconductor device, comprising:

a plurality of banks each having multiport
20 memory cells for transferring data of each memory cell through a single bit line in accordance with a single-end scheme; and

read means that is interposed between said banks for supplying as output to the outside data that
25 have been read to a single bit line for each of said banks;

. said read means including:

a differential sense amplifier for comparing
said data that are transferred with a reference signal
when a determination start signal, which is synchronized
5 with a word line signal, for determining whether or not
said data are to be transferred is in an active state;

a clocked inverter for receiving as input said
data that are supplied from said differential sense
amplifier and supplying said data as output when said
10 determination start signal is in an active state;

discharging means for discharging the lower-
order bit line in accordance with the output result of
said clocked inverter; and

discharge prevention means for preventing the
15 discharging operation of said discharging means and
holding the input of said clocked inverter at a
precharged potential when said determination start signal
is in an inactive state;

whereby a control operation, based on the
20 output result of said clocked inverter in said
determination means of this bank, for determining whether
data transfer by said read means in the succeeding bank
is allowed, is successively executed, as far as the
lowest-order bank, to thereby perform desired data
25 transfer.

9. A data read circuit according to claim 3,
wherein said read means includes:

a single bit line that is selectively
precharged by a precharging transistor and a precharge
5 holding transistor that is connected in parallel with
said precharging transistor;

a NOR circuit having its input terminal
connected to said bit line and the signal line of said
determination start signal, and its output terminal
10 connected to the gate electrode of said precharge holding
transistor; and

a discharging transistor having its gate
electrode connected to the output terminal of said NOR
circuit, its drain electrode connected to said lower-
15 order bit line, and its source electrode connected to the
ground potential.

10. A data read circuit according to claim 4,
wherein said read means includes:

20 a single bit line that is selectively
precharged by a precharging transistor and a precharge
holding transistor that is connected in parallel with
said precharging transistor;

a clocked inverter having its data input
25 terminal connected to said bit line, one of its clock
input terminals connected to the determination start

signal, the other of its clock input terminals connected to a polarity-inverted signal of said determination start signal, and its output terminal connected to the gate electrode of said precharge holding transistor;

5 an output holding transistor having its drain electrode connected to the output terminal of said clocked inverter, its source electrode connected to ground, and its gate electrode connected to the polarity-inverted signal of said determination start signal; and

10 a discharging transistor having its gate electrode connected to the output terminal of said clocked inverter, its drain electrode connected to said lower-order bit line, and its source electrode connected to ground.

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11. A data read circuit according to claim 5, wherein said read means includes:

 a single bit line that is selectively precharged by a precharging transistor and a precharge
20 holding transistor that is connected in parallel with said precharging transistor;

 a clocked inverter having its data input terminal connected to said bit line, one of its clock input terminals connected to the determination start
25 signal, the other of its clock input terminals connected to a polarity-inverted signal of said determination start

signal, and its output terminal connected to the gate electrode of said precharge holding transistor;

an output holding transistor having its drain electrode connected to the output terminal of said

5 clocked inverter, its source electrode connected to ground, and its gate electrode connected to the polarity-inverted signal of said determination start signal; and

a discharging transistor having its gate electrode connected to the output terminal of said

10 clocked inverter, its drain electrode connected to said lower-order bit line, and its source electrode connected to ground.

12. A data read circuit according to claim 6,
15 wherein said read means includes:

a single bit line for being selectively precharged by a precharging transistor and a precharge holding transistor connected in parallel with said precharging transistor;

20 a voltage comparator having its positive input terminal connected to said bit line, its negative input terminal connected to a reference signal line, and its control terminal connected to a determination start signal line;

25 a clocked inverter having its data input terminal connected to the output terminal of said voltage

comparator, one of its clock input terminals connected to said determination start signal, the other of its clock input terminals connected to the polarity-inverted signal of said determination start signal; and its output
5 terminal connected to the gate electrode of said precharge holding transistor;

an output holding transistor having its drain electrode connected to the output terminal of said clocked inverter, its source electrode connected to the
10 ground potential, and its gate electrode connected to the polarity-inverted signal of said determination start signal; and

a discharging transistor having its gate electrode connected to the output terminal of said
15 clocked inverter, its drain electrode connected to said lower-order bit line, and its source electrode connected to the ground potential.

13. A data read circuit according to claim 9,
20 wherein the drive capability of said discharging transistor is preset to a level that equals or surpasses the drive capability of said plurality of circuit blocks.

14. A data read circuit according to claim 10,
25 wherein the drive capability of said discharging transistor is preset to a level that equals or surpasses

the drive capability of said plurality of circuit blocks.

15. A data read circuit according to claim 11,
wherein the drive capability of said discharging
5 transistor is preset to a level that equals or surpasses
the drive capability of said plurality of circuit blocks.

16. A data read circuit according to claim 12,
wherein the drive capability of said discharging
10 transistor is preset to a level that equals or surpasses
the drive capability of said plurality of circuit blocks.